Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.019”**

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**.019”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .003 X .004” min.**

**Backside Potential: Collector**

**Mask Ref: STL**

**APPROVED BY: DK DIE SIZE .019” X .019” DATE: 1/26/22**

**MFG: ALLEGRO / SPRAGUE THICKNESS .006” P/N: 2N3798**

**DG 10.1.2**

#### Rev B, 7/19/02